IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claim 2 and AMEND claims 1, 8 and 11 in accordance with the following:

1. (CURRENTLY AMENDED) A microcontroller operating in synchronization with a clock, comprising:

an arithmetic unit operating in synchronization with the clock;

an internal resource ~~being~~ connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit both of which ~~operates~~ operate in synchronization with the clock; and

a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock (m =< n), and supplies the operation permission signal to the internal circuit of the internal resource,

wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state.

2. (CANCELLED)

3. (ORIGINAL) The microcontroller according to claim 1,

wherein the internal resource includes a communication macro controlling communication with outside, and an internal circuit of the communication macro includes a counter which generates a communication control clock.

4. (ORIGINAL) The microcontroller according to claim 1,

wherein the internal resource comprises a pulse generation macro generating a control pulse, and an internal circuit of the pulse generation macro comprises a counter controlling a generation timing of the control pulse.

5. (ORIGINAL) The microcontroller according to claim 1,

wherein the system resource prescaler comprises a register storing the values m and n, and the register can be set alterably.

6. (ORIGINAL) The microcontroller according to claim 5,

wherein the system resource prescaler comprises a settable operation control register indicative of either a first operation state in which the operation permission signal is set constantly to the operation permission state or a second operation state in which the operation permission signal is set to the operation permission state in the m cycles out of the n cycles.

7. (ORIGINAL) The microcontroller according to claim 1,

wherein the system resource prescaler dispersively allocates the m cycles throughout the n cycles.

8. (CURRENTLY AMENDED) The microcontroller ~~according to claim 1,~~operating in synchronization with a clock, comprising:

an arithmetic unit operating in synchronization with the clock;

an internal resource being connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit both of which operates in synchronization with the clock; and

a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock (m =<n), and supplies the operation permission signal to the international circuit of the internal resource,

wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state,

wherein the system resource prescaler comprises a preceding-stage prescaler and a succeeding-stage prescaler which generates a succeeding-stage operation permission signal using a preceding-stage operation permission signal which is generated and supplied from the preceding-stage prescaler, and the succeeding-stage operation permission signal is supplied to the internal circuit of the internal resource.

9. (ORIGINAL) The microcontroller according to claim 8,

wherein the preceding-stage prescaler and the succeeding-stage prescaler respectively comprise registers storing the values m and n, and the registers can be set alterably.

10. (ORIGINAL) The microcontroller according to claim 9,

wherein the succeeding-stage prescaler further comprises an operation control register in which can be set any one of a first operation state enabling the succeeding-stage operation permission signal to be set constantly to an operation permission state, a second operation state enabling the succeeding-stage operation permission signal to be set to the operation permission state in the m cycles out of the n cycles, and a third state generating the succeeding-stage operation permission signal irrespective of the states of the preceding-stage operation permission signal.

11. (CURRENTLY AMENDED) A microcontroller operating in synchronization with a clock, comprising:

an arithmetic unit operating in synchronization with the clock;

an internal resource being connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit both of which ~~operating~~ operate in synchronization with the clock; and

a system resource prescaler which generates, from the clock, an operation permission signal having a lower frequency than the clock, and supplies the operation permission signal to the internal circuit of the internal resource,

wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state.

12. (ORIGINAL) The microcontroller according to claim 11,

wherein the operation permission signal is controlled to be set to the operation permission state on a cycle-by-cycle basis of the clock.

13. (ORIGINAL) The microcontroller according to claim 12,

wherein the operation permission signal is set to the operation permission state in m cycles out of n cycles of the clock, and the values n and m can be set alterably.